ABSTRACT OF THE DISCLOSURE

A thin film transistor and its fabrication method. The transistor includes a buffer layer on a substrate, and a poly-crystalline semiconductor layer on the buffer layer. The poly-crystalline semiconductor layer includes a channel layer, offset regions along sides of the channel layer, sequential doping regions along sides of the offset regions, and source and drain regions. The doping concentration is sequentially changed in the sequential doping region. A sloped gate insulation layer is on the poly-crystalline semiconductor layer. A gate electrode having a main gate electrode and auxiliary gate electrodes is on the sloped insulation layer. An interlayer is over the gate electrode and source and drain electrodes are formed in contact with the source and drain regions and on the interlayer. The poly-crystalline semiconductor layer is formed by ion doping a poly-crystalline semiconductor layer through the gate insulation layer while using the gate electrode as a mask.